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PATENT
Reply under 37 CFR 1.116
EXPEDITED PROCEDURE
Group 2121

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of)
Michael A. Marra et al.) Group: 2121
Serial No.: 09/226,971)
Filed: January 8, 1999)
Title: METHOD OF REGULATING A TARGET)
SYSTEM USING A FREQUENCY)
COMPARISON OF FEEDBACK AND)
REFERENCE PULSE TRAINS)
Examiner: B. Garland

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AMENDMENT TRANSMITTAL SHEET

Box AF
Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated as follows:

CLAIMS AS AMENDED						
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE
TOTAL CLAIMS	8	MINUS	20	0	x \$ 9 x \$18	0.00
INDEPENDENT CLAIMS	4	MINUS	4	1	x \$40 x \$80	0.00
FEE FOR MULTIPLE CLAIMS \$130/\$260						
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						\$0.00

[] Verified Statement claiming small entity status is enclosed, if not filed previously.
[] A check in the amount of \$ _____ is enclosed to cover the additional fees.
[] A check in the amount of \$ _____ to cover the Extension fee for response within the _____ month is enclosed.

Respectfully submitted,

Todd T. Taylor
Attorney for Applicant

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THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Michael A. Marra et al.
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Group: 2121
)
)
Examiner: S. R. Garland

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REQUEST FOR RECONSIDERATION

Box AF
Commissioner for Patents
Washington, D.C. 20231

Sir:

Responsive to the Final Office Action dated July 26, 2001, Applicant hereby submits the following Request for Reconsideration.

REMARKS

Claims 1-8 are pending in this application. Claims 1-3, 5 and 8 are rejected; and claims 4, 6 and 7 are allowed.

Responsive to the rejection of claims 1 and 8 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,212,434 (Hsieh), Applicants respectfully traverse the rejection and submit that claims 1 and 8 are in condition for allowance.

Hsieh discloses a phase-locked step motor speed servo controller, including motor 50, speed detector 60 and phase detector 10. Phase detector 10 has a first input port V, a second input port R, an output $V_1(t)$ and a phase error output θ_e . First input port V is connected to the output of speed detector 60 to receive feedback signal $P_1(t)$ having phase θ_1 and second input port